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10/533,400	04/25/2005	Andrea Bragagnini	23279	9081

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EXAMINER	
PARTRIDGE, WILLIAM B	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 10/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/533,400	BRAGAGNINI ET AL.	
	Examiner	Art Unit	
	William B. Partridge	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/25/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-42 are pending and have been examined.

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on April 25th, 2005. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

2. Claims 1-3, 5-12, 14-18, 21-24, 26-33, 35-39 and 42 are objected to because of the following informalities:

As per claims 1-3, 5-12, 14-18, 21-24, 26-33, 35-39 and 42, they include numbering referring to drawings.

As per claim 18, lines 3-4, "said at least computational block" should be "said at least one computational block".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 9 and 22-42 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As per claim 9, Applicant discloses the reset of a state register and the state register being capable of re-cycling through the same value. However, it is unclear as to how these functions are performed as there is no description of these capabilities in the disclosure

As per claims 22-42, Applicant discloses the method of executing a state machine. However, there appears to be no disclosure as to how the state machine is executed.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 22-42 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 22-42 are claiming a method for execution but only describe the architecture of the system and not how things are executed on said system.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-4, 6-8, 10-12, 21-25, 27-29, 31-33, and 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Burrows et al. (5,125,098).

Claim 1

Burrows discloses:

An architecture for a state machine with a number of states of the machine, the architecture including a memory having a set of addresses, wherein said memory is arranged to store at each of said addresses in the set the complete description of a respective one of said number of states of the machine (Column 3 lines 8-28, FIG 3).

Claim 2

The rejection of claim 1 is incorporated and further Burrows discloses:

said memory is clocked by a clock signal and in that said memory is arranged to switch from one state to another state within a single cycle of said clock signal (Column 3 lines 8-28, FIG 3). The latch contains the next state, or new current state, and loads the value upon clocking.

Claim 3

The rejection of claim 1 is incorporated and further Burrows discloses:

said memory comprises at each address in said set a plurality of memory units adapted to be simultaneously selected to store a respective portion of said complete description of said respective one of said number of states of the machine (Column 3 lines 8-28, FIG 3). Each memory location has an output that will be generated upon selection of said location. While CAM is being used it is also noted that RAM could be used (Column 3 lines 53-55) and is only used for size advantages.

Claim 4

The rejection of claim 3 is incorporated and further Burrows discloses:

said plurality of memory units are mapped on an address plane with memory cells of a given length (FIG 3). As illustrated in FIG 3 the size of the memory is defined and as such the size of the memory cells is defined as well.

Claim 6

The rejection of claim 1 is incorporated and further Burrows discloses:

said number of states of the machine are expressed as binary values, (Column 2 line 35).

and transitions between states of said number of states take place between a present state and a next state (Column 3 lines 8-28, FIG 3). The next state is determined based on the previous next state, the current state, and inputs.

Claim 7

The rejection of claim 6 is incorporated and further Burrows discloses:

the binary value for said next state is used to re-address said memory (Column 3 lines 8-28, FIG 3).

Claim 8

The rejection of claim 6 is incorporated and further Burrows discloses:

a state register to contain the binary value for said present state, said state register being adapted to address said memory (Column 3 lines 8-28, FIG 3). A register and a latch are both made of flip-flops. It is inherent that the use of a register is interchangeable of that of a latch.

Claim 10

The rejection of claim 1 is incorporated and further Burrows discloses:

a controller having a respective input line (EAB) to the state machine, said controller being arranged to selectively feed said memory with re-programming signals received over said respective input line (Column 3 lines 8-28, FIG 3). The latch and multiplexer function together as a controller.

Claim 11

The rejection of claim 10 is incorporated and further Burrows discloses:

an output and state selector having a set of input lines (IS) to the machine and in that said respective input line to said controller is distinct from said input (IS) lines of said selector (Column 3 lines 8-28, FIG 3).

Claim 12

The rejection of claim 1 is incorporated and further Burrows discloses:

an output and state selector having a set of input lines (IS) to the machine and in that said selector comprises at least one line in said set of input lines (IS) adapted to receive input signals as two bit condition signals whereby said condition can be expressed as a three state signal (1,0,X) (Column 4 lines 64-68, FIG 3).

Claim 21

The rejection of claim 1 is incorporated and further Burrows discloses:

said memory (14) is a random access memory (RAM) (Column 3 lines 53-55). While CAM is being used it is also noted that RAM could be used and is only used for size advantages.

Claims 22-25, 27-29, 31-33, and 42

Claims 22-25, 27-29, 31-33, and 42 are the method claims corresponding to the architecture claims 1-4, 6-8, 10-12, and 21 respectively, and are rejected under the

same reasons set forth in connection with the rejections of claims 1-4, 6-8, 10-12, and 21.

9. Claims 1-7, 10-16, 21-28, 31-37, and 42 are rejected under 35 U.S.C. 102(b) as being anticipated by O'Connor (5,905,902).

Claim 1

O'Connor discloses:

An architecture for a state machine with a number of states of the machine, the architecture including a memory having a set of addresses, wherein said memory is arranged to store at each of said addresses in the set the complete description of a respective one of said number of states of the machine (FIG 2).

Claim 2

The rejection of claim 1 is incorporated and further O'Connor discloses:

said memory is clocked by a clock signal and in that said memory is arranged to switch from one state to another state within a single cycle of said clock signal (Column 6 lines 59-61).

Claim 3

The rejection of claim 1 is incorporated and further O'Connor discloses:

said memory comprises at each address in said set a plurality of memory units adapted to be simultaneously selected to store a respective portion of said

complete description of said respective one of said number of states of the machine (FIG 3).

Claim 4

The rejection of claim 3 is incorporated and further O'Connor discloses:

said plurality of memory units are mapped on an address plane with memory cells of a given length (FIG 3).

Claim 5

The rejection of claim 1 is incorporated and further O'Connor discloses:

said complete description of a respective one of said number of states of the machine is partitioned in a number of sections, each said section describing a possible transition from said respective one state towards another state of said number of states of the machine (FIG 3).

Claim 6

The rejection of claim 1 is incorporated and further O'Connor discloses:

said number of states of the machine are expressed as binary values, (FIG 4).

and transitions between states of said number of states take place between a present state and a next state (FIG 2-3).

Claim 7

The rejection of claim 6 is incorporated and further O'Connor discloses:

the binary value for said next state is used to re-address said memory (FIG 2).

Claim 10

The rejection of claim 1 is incorporated and further O'Connor discloses:

a controller having a respective input line (EAB) to the state machine, said controller being arranged to selectively feed said memory with re-programming signals received over said respective input line (Column 4 lines 35-59, FIG 5).

Claim 11

The rejection of claim 10 is incorporated and further O'Connor discloses:

an output and state selector having a set of input lines (IS) to the machine and in that said respective input line to said controller is distinct from said input (IS) lines of said selector (FIGS 5-7).

Claim 12

The rejection of claim 1 is incorporated and further O'Connor discloses:

an output and state selector having a set of input lines (IS) to the machine and in that said selector comprises at least one line in said set of input lines (IS)

adapted to receive input signals as two bit condition signals whereby said condition can be expressed as a three state signal (1,0,X) (Column 8 lines 1-14).

Claim 13

The rejection of claim 1 is incorporated and further O'Connor discloses:

a default transition is provided among states of said number of states, said default transition including said next state as well as the values of said output signals (OS) (Column 8 lines 40-52, FIG 9).

Claim 14

The rejection of claim 13 is incorporated and further O'Connor discloses:

said machine is arranged to select said default transition when none of the conditions on the inputs of the other transitions is met (Column 8 lines 40-52, FIG 9).

Claim 15

The rejection of claim 13 is incorporated and further O'Connor discloses:

said machine (10) is a Moore machine and in that to each said transition there correspond the output values of said default transition (Column 8 lines 40-52, FIG 9). A Moore machine is common knowledge to one of ordinary skill in the art and is inherent.

Claim 16

The rejection of claim 6 is incorporated and further O'Connor discloses:

an output and state selector having a set of input lines (IS) to the machine, said selector including a plurality of comparators, each of said comparators being adapted to receive over said set of input lines (IS) input signals as well as one of the possible input configurations described in the state description; said selector being arranged to select a next state of said number of states as well as the corresponding set of output signals (OS) if one of said comparators provides a positive result, default values being selected in the absence of any such positive result (Column 8 lines 40-52, FIGS 7-9).

Claim 21

The rejection of claim 1 is incorporated and further O'Connor discloses:

said memory (14) is a random access memory (RAM) (Column 3 lines 6-9, FIG 2).

Claims 22-28, 31-37, and 42

Claims 22-28, 31-37, and 42 are the method claims corresponding to the architecture claims 1-7, 10-16, and 21 respectively, and are rejected under the same reasons set forth in connection with the rejections of claims 1-7, 10-16, and 21.

10. Claims 1-3, 6-8, 10, 21-24, 27-29, 31, 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Shelton et al. (5,825,199).

Claim 1

Shelton discloses:

An architecture for a state machine with a number of states of the machine, the architecture including a memory having a set of addresses, wherein said memory is arranged to store at each of said addresses in the set the complete description of a respective one of said number of states of the machine (Column 5 lines 5-15, FIG 2).

Claim 2

The rejection of claim 1 is incorporated and further Shelton discloses:

said memory is clocked by a clock signal and in that said memory is arranged to switch from one state to another state within a single cycle of said clock signal (Column 4 lines 5-16, FIG 2).

Claim 3

The rejection of claim 1 is incorporated and further Shelton discloses:

said memory comprises at each address in said set a plurality of memory units adapted to be simultaneously selected to store a respective portion of said complete description of said respective one of said number of states of the machine (Column 4 line 51 – Column 5 line 15, FIG 2).

Claim 6

The rejection of claim 1 is incorporated and further Shelton discloses:

said number of states of the machine are expressed as binary values, (FIG 2). RAM and ROM are used to store state values and as such the values are inherently binary values.

and transitions between states of said number of states take place between a present state and a next state (Column 2 lines 11-38, FIG 2).

Claim 7

The rejection of claim 6 is incorporated and further Shelton discloses:

the binary value for said next state is used to re-address said memory (Column 4 lines 5-16, FIG 2). The current state is used to select the next state from the logic array that obtains its data from either ROM or RAM.

Claim 8

The rejection of claim 6 is incorporated and further Shelton discloses:

a state register to contain the binary value for said present state, said state register being adapted to address said memory (Column 4 lines 5-16, FIG 2).

Claim 10

The rejection of claim 1 is incorporated and further Shelton discloses:

a controller having a respective input line (EAB) to the state machine, said controller being arranged to selectively feed said memory with re-programming signals received over said respective input line (Column 5 lines 16-21, FIG 2). The controller selects the use of RAM or ROM. It is inherent that the RAM disclosed can be reprogrammed

Claim 21

The rejection of claim 1 is incorporated and further Shelton discloses:

said memory (14) is a random access memory (RAM) (FIG 2).

Claims 22-24, 27-29, 31, and 42

Claims 22-24, 27-29, 31, and 42 are the method claims corresponding to the architecture claims 1-3, 6-8, 10, and 21 respectively, and are rejected under the same reasons set forth in connection with the rejections of claims 1-3, 6-8, 10, and 21.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 9 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shelton et al. (5,825,199) in view of Bailey et al. (5,461,649).

Claim 9

The rejection of claim 8 is incorporated and further Shelton discloses:

a controller to control access to said memory, (Column 5 lines 16-21, FIG 2)

said controller being arranged to perform at least one of the functions selected from the group consisting of: causing said memory to be addressed via said state register, (Column 4 lines 5-16, FIG 2)

Shelton does not specifically disclose:

reset the contents of said state register, causing said state register to re-cycle through the same binary value. However, Bailey, in an analogous art, discloses the above limitation (Abstract, FIG 5).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Bailey into the teaching of Shelton to have a reset and recycle option. The modification would have been obvious because one of ordinary skill in the art would have been motivated to provide a reset option in order to allow for an easy restart of the state machine and to have a recycle function to eliminate keeping extra state information in memory. Both features would allow for a smaller memory size.

Claim 30

Claim 30 is the method claims corresponding to the architecture claim 9, and is rejected under the same reasons set forth in connection with the rejection of claim 9.

13. Claims 17-20 and 38-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burrows et al. (5,125,098) in view of Wolf (The FSM network model for behavioral synthesis of control-dominated machines).

Claim 17

The rejection of claim 1 is incorporated but Burrows does not specifically disclose:

a plurality of counters for describing the state machine, said counters being provided as external components of said state machine, said counters being arranged to communicate with the said state machine by means of at least one of an enable signal and an end-of-count signal. However, Wolf, in an analogous art, discloses the above limitation (FIG 4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Wolf into the teaching of Burrows to have an external counter for control. The modification would have been obvious because one of ordinary skill in the art would have been motivated provide control external to the state machine to be able to modify the loop count without reprogramming the entire state machine logic.

Claim 18

The rejection of claim 1 is incorporated but Burrows does not specifically disclose:

at least one computational block external with respect to said state machine, said at least computational block being arranged to communicate with said state machine by means of at least one signal selected from the group

consisting of the signals input to the machine (IS) and the signals output from the machine (OS). However, Wolf, in an analogous art, discloses the above limitation (FIG 4; As per Applicant's disclosure a counter is just a computational block).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Wolf into the teaching of Burrows to have an external computational block for control. The modification would have been obvious because one of ordinary skill in the art would have been motivated provide control external to the state machine to be able to modify the loop count without reprogramming the entire state machine logic.

Claim 19

The rejection of claim 17 is incorporated and further Wolf discloses:

said counters have at least one of a reference value and an end-of-count value, said counters being arranged so that said at least one of said reference value and said end-of-count value can be modified run time (FIG 4). Counters inherently, by their nature, can have a programmed start value and an overflow value. The values could be modified as either a count up or count down and an initial value from which to count from.

Claim 20

The rejection of claim 17 is incorporated and further wolf discloses:

said counters comprise at least one re-writable register adapted to contain a reference value for the respective counter (FIG 4). Counters inherently have registers in order to store the initial value.

Claims 38-41

Claims 38-41 are the method claims corresponding to the architecture claims 17-20 respectively, and are rejected under the same reasons set forth in connection with the rejections of claims 38-41.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Bosch (4,370,729) teaches a microprogram sequencer for generating in a sequence the address of microinstructions.

Russell (6,212,625) teaches a dynamically programmable state engine for executing finite state machines.

Gabris et al. (4,755,967) teaches a programmable synchronous sequential state machine or sequencer having decision variable input mapping circuit responsive to feedback signals.

Sachs (2003/0140218) teaches a state machine.

Lemay et al. (5,280,595) teaches a state machine for executing commands within a minimum number of cycles.

Ziobro (4,407,015) teaches a multiple event driven micro-sequencer.

Vermeulen et al. (Flexible hardware acceleration for multimedia oriented microprocessors) teaches a finite state machine with looping.

Larus (The SPIM Simulator for the MIPS R2000/R3000) teaches finite state machine control and memory hierarchies.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William B. Partridge whose telephone number is (571) 270-1402. The examiner can normally be reached on M-TR 7:30 - 5:00, alternate F 7:30 - 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chameli Das can be reached on (571) 272-3696. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Chameli C Das

CHAMELI DAS
SUPERVISORY PATENT EXAMINER

10/16/06.

Examiner: William B Partridge
Date: October 13th, 2006